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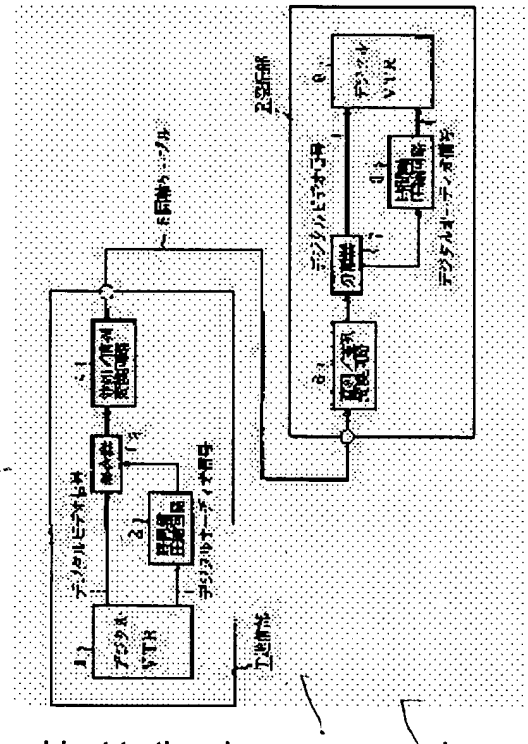
(54) TRANSMISSION METHOD, TRANSMITTER AND TIME BASE EXPANDER FOR DIGITAL VIDEO SIGNAL AND DIGITAL AUDIO SIGNAL

(57)Abstract:

PURPOSE: To provide a transmission method for a digital video signal and a digital audio signal with a simple configuration and ease of handling in which the digital video signal and the digital audio signal are simultaneously transmitted through the use of a few number of cables.

CONSTITUTION: A transmission section T applies time base compression to a digital audio signal and the result is mixed in a digital video signal so as to be inserted in a horizontal synchronization tip period, the mixed digital video/audio signal is parallel/serial-converted and the converted signal is sent to a reception section R through one cable 5, the reception section R applies serial/parallel-conversion to the serial digital video/audio signal, the digital video signal and the digital audio signal subject to time base compression are separated from the digital video/audio signal and the digital audio signal subject to time base compression is expanded with respect to the time base.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] In the transmitting section, carry out time base compaction of the digital audio signal, and mix and parallel/serial conversion of the digital video/the audio signal this mixed is carried out so that it may insert in the horizontal synchronization chip period of a digital video signal. Transmit to a receive section through one cable, and the above-mentioned serial digital video / audio signal are carried out a serial/parallel conversion in this receive section. The transmission approach of of the digital video signal and digital audio signal which are characterized by separating a digital video signal and the digital audio signal by which time base compaction was carried out from this juxtaposition digital video / audio signal, and carrying out time-axis expanding of this digital audio signal by which time base compaction was carried out.
[Claim 2] The time-base-compaction circuit which carries out time base compaction of the digital audio signal, and the mixing circuit which inserts in the horizontal synchronization chip period of a digital video signal the digital audio signal by which time base compaction was carried out from this time-base-compaction circuit, The transmitting section equipped with the parallel/serial-conversion circuit to which the juxtaposition digital video / audio signal from this mixing circuit are supplied, The serial / parallel-conversion circuit to which the serial digital video / audio signal transmitted through one cable from the parallel/serial-conversion circuit of the above-mentioned transmitting section are supplied, The separation circuit which the juxtaposition digital video / audio signal from this serial / parallel-conversion circuit are supplied, and is divided into a digital video signal and the digital audio signal by which time base compaction was carried out, Transmission equipment of the digital video signal characterized by having a receive section having the time-axis expanding circuit to which the digital audio signal by which time base compaction was carried out from this separation circuit is supplied, and a digital audio signal.
[Claim 3] The memory to which reading appearance of the output data with which the input data was written in and time-axis expanding of it was carried out is carried out, The write-in address generation circuit which writes in this memory and supplies an address signal, The read-out address generation circuit which reads to the above-mentioned memory and supplies an address signal, The read-out address signal from the above-mentioned read-out address generation circuit is compared with the write-in address signal from the above-mentioned write-in address generation circuit. The comparison circuit which controls the above-mentioned read-out address generation circuit so that the above-mentioned read-out address does not cross the above-mentioned write-in address, The read-out address signal from the above-mentioned read-out address generation circuit is compared with the read-out address signal from the above-mentioned write-in address generation circuit. Time-axis expanding equipment characterized by having the time delay convergence circuit which controls the above-mentioned read-out address generation circuit so that the above-mentioned read-out address approaches the above-mentioned write-in address.
[Claim 4] The above-mentioned reading appearance of the above-mentioned time delay convergence circuit is carried out from the write-in address signal from the above-mentioned write-in address

generation circuit. with the subtractor from a address generation circuit which carries out reading appearance and subtracts an address signal When the output of the above-mentioned predetermined period above-mentioned subtractor is forward based on the output from the positive/negative decision circuit which makes a predetermined period judgment of the positive/negative of the output of this subtractor, and this positive/negative decision circuit, the above-mentioned reading appearance -- carrying out -- the initial address of a address generation circuit -- this -- size -- the time-axis expanding equipment according to claim 3 characterized by setting it as the predetermined address.

[Claim 5] The memory to which the data of two or more channels are repeatedly written one by one, and repeat reading appearance of the data of two or more channels by which time-axis expanding was carried out is carried out one by one, Two or more write-in address generation circuits which generate the write-in address signal for every above-mentioned two or more channels, and are supplied to the above-mentioned memory, The maximum write-in address generation circuit which generates the maximum write-in address signal for every round of the above-mentioned two or more channels among each write-in address of two or more above-mentioned write-in address generation circuits, Reading appearance is carried out. reading appearance is carried out, an address signal is generated, and the above-mentioned memory is supplied -- with a address generation circuit The read-out address signal from the above-mentioned read-out address generation circuit is compared with the maximum write-in address signal from the above-mentioned maximum write-in address generation circuit. Time-axis expanding equipment characterized by having the comparison circuit which controls the above-mentioned read-out address generation circuit so that the above-mentioned read-out address does not cross the above-mentioned maximum write-in address.

[Claim 6] the time-axis expanding equipment according to claim 5 carry out above-mentioned reading appearance, carry out the reading appearance of this write-in address signal, and will carry out having prepared the change circuit from a address generation circuit which carries out change supply at the above-mentioned memory as the description as an address signal in the above-mentioned comparison circuit if reading appearance carries out, the above-mentioned reading appearance of the address signal carries out as compared with each write-in address signal from that of two or more above-mentioned write-in address generation circuits, a address generation circuit carries out reading appearance and the address crosses one write-in address of two or more above-mentioned write-in address generation circuits.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to time-axis expanding equipment at the transmission system and transmission equipment list of a digital video signal and a digital audio signal.
[0002]
[Description of the Prior Art] It has changed so that a serial transmission may be adopted as the effective transmission approach of a digital video signal with the spread of digital VTR in recent years. When a digital audio signal was conventionally transmitted with a digital video signal, a total of one cable for transmitting a digital video signal, two cables for transmitting a digital audio signal, and three cables was needed.
[0003]
[Problem(s) to be Solved by the Invention] Since a total of no less than three cables was required of the transmission approach of transmitting simultaneously a conventional digital video signal and a conventional digital audio signal, the configuration was complicated and handling was troublesome.
[0004] In view of this point, the 1st object of this invention can transmit simultaneously a digital video signal and a digital audio signal using the cable of a small number, a configuration is easy, and it is offering the transmission approach of of the digital video signal and digital audio signal to which handling becomes easy, and transmission equipment.
[0005] The transmission equipment and the transmission approach of this digital video signal and a digital audio signal to a receive section so that it may mention later time-axis expanding circuit ****** The measurement size of the digital audio signal currently mixed by the digital video signal for every level line is not fixed, or Although it is necessary to enlarge the window of the memory used in a time-axis expanding circuit in order to absorb the heterogeneity of the measurement size of the digital audio signal for every level line of the digital video signal, when the number of channels of the digital audio signal is not fixed If it is made such, after the digital audio signal by which time base compaction was carried out will be written in memory, reading appearance will be carried out, delay of until will change greatly, or indefinite width of face of delay will be enlarged. Therefore, he makes the window of the memory small as much as possible, and was trying for the amount of delay and indefinite width of face to change small in the conventional time-axis expanding circuit.
[0006] Since data are come to memory also by the 2nd object of this invention not making a window not much small, either in view of this point, it is offering the time-axis expanding equipment which can shorten the time delay to data reading **** by which time-axis expanding was carried out.
[0007] By the way, it is mixed so that time base compaction may be carried out within the horizontal synchronization chip period of a digital video signal and it may insert. In the case of four channels, the digital audio signal transmitted to a receive section R through a coaxial cable 5 from the transmitting section T the samples CH1, CH2, CH3, and CH4 of the audio signal of four channels ..... CH1, CH2, CH3, CH4, CH1, CH2, CH3, CH4, CH1, CH2, CH3, CH4, ... **, although it is satisfactory when sequential transmission is carried out like CH2, CH4, CH3, CH1, CH2, CH4, CH3, CH1,

CH2, CH4, CH3, CH1 ..... ** -- sequence being [like] out of order, or ..... CH2, CH4, CH2, CH4, CH2, CH4, CH2, CH4, CH2, CH4, CH2, CH4 When the sample of the audio signal of some channels is missing like ....., control of the writing in the memory of a time-axis expanding circuit and the read-out address will not be able to be **(ed), and it will change.

[0008] in view of this point , the digital audio signal of two or more channels be supply , and in the time-axis expanding equipment with which the digital audio signal of two or more channels by which time-axis expanding be carried out be output , the 3rd object of this invention be offer what can perform smoothly control of a write-in address register and a read-out address register , even if it lack the sample of some channels of the digital audio signal of two or more channels which be going to carry out time-axis expanding or sequence be wrong .

[0009] Moreover, it is mixed so that time base compaction may be carried out within the horizontal synchronization chip period of a digital video signal and it may insert. In the case of four channels, the digital audio signal transmitted to a receive section R through a coaxial cable 5 from the transmitting section T the samples CH1, CH2, CH3, and CH4 of the audio signal of four channels ..... CH1, CH2, CH3, CH4, CH1, CH2, CH3, CH4, CH1, CH2, CH3, CH4 although it is satisfactory when sequential transmission is carried out like ....., ..., CH2, CH4, CH2, CH4, CH2, CH4 and a period with the sample of the channel which exists like .... are not lacking, or one sample is also no longer sent in the middle of transmission -- this -- ** -- it is.

[0010] Then, the write-in address register and the maximum write-in address register for every channel are prepared so that it may mention later. And carry out reading appearance, an address register carries out reading appearance, and the address is compared. reading appearance -- carrying out -- the time -- writing in -- the write-in address of an address register -- Read, only when the write-in address reads and it consists of the address with size, make the read-out address of an address register increase, and when that is not right, according to the time-axis expanding equipment it was made to stop an increment, the read-out address Although control of the write-in address of a write-in address register and a read-out address register and the read-out address changes possible Since the increment in the read-out address of a read-out address register is also stopped when the increment in the maximum write-in address of a maximum write-in address register stops, there is a possibility that the sample data of a right digital audio signal cannot be then read from memory.

[0011] In the time-axis expanding equipment with which, as for the 4th object of this invention, the digital audio signal of two or more channels is supplied, and the digital audio signal of two or more channels by which time-axis expanding was carried out is outputted in view of this point Even if it lacks a part of sample of the digital audio signal of two or more channels or sequence is wrong, while being able to perform smoothly control of a write-in address register and a read-out address register Even if the increment in the maximum write-in address of a maximum write-in address counter stops, it is offering the time-axis expanding equipment which can read certainly the required data memorized by memory, can maintain the continuity of data, and can perform the faithful rendering of received data.

[0012]

[Means for Solving the Problem and its Function] The transmission approach of the digital video signal by the 1st this invention, and a digital audio signal Carry out time base compaction of the digital audio signal in the transmitting section T, mix so that it may insert in the horizontal synchronization chip period of a digital video signal, and parallel/serial conversion of the mixed its digital video/the audio signal is carried out. Transmit to a receive section R through one cable 5, and a serial digital video / audio signal is carried out a serial/parallel conversion in the receive section R. A digital video signal and the digital audio signal by which time base compaction was carried out are separated from its juxtaposition digital video / audio signal, and it is made to carry out time-axis expanding of the digital audio signal by which time base compaction was carried out.

[0013] The transmission equipment of the digital video signal by the 2nd this invention, and a digital audio signal The time-base-compaction circuit 2 which carries out time base compaction of the digital audio signal, and the mixing circuit 3 which inserts in the horizontal synchronization chip period of a digital video signal the digital audio signal by which time base compaction was carried out from the

time-base-compaction circuit 2, The transmitting section T equipped with the parallel/serial-conversion circuit 4 to which the juxtaposition digital video / audio signal from the mixing circuit 3 are supplied The serial / parallel-conversion circuit 6 to which the serial digital video / audio signal transmitted through one cable 5 from the parallel/serial-conversion circuit 4 of the transmitting section T are supplied, The separation circuit 7 which the juxtaposition digital video / audio signal from its serial / parallel-conversion circuit 6 are supplied, and is divided into a digital video signal and the digital audio signal by which time base compaction was carried out, It has the receive section R having the time-axis expanding circuit 8 to which the digital audio signal by which time base compaction was carried out from the separation circuit 7 is supplied.

[0014] According to this 2nd this invention, time base compaction of the digital audio signal is carried out by the time-base-compaction circuit 2 in the transmitting section T. Mix so that it may insert in the horizontal synchronization chip period of a digital video signal with a mixer 3, and parallel/serial conversion of the mixed its juxtaposition digital video / the audio signal is carried out by the parallel/serial-conversion circuit 4. Transmit to a receive section R through one cable 5, and a serial digital video / audio signal is carried out a serial/parallel conversion by the serial / parallel-conversion circuit 6 in the receive section R. An eliminator 7 separates into a digital video signal and the digital audio signal by which time base compaction was carried out from its juxtaposition digital video / audio signal, and time-axis expanding of the digital audio signal by which time base compaction was carried out is carried out by the time-axis expanding circuit 8.

[0015] The memory 11 to which reading appearance of the output data with which the input data was written in by the time-axis expanding equipment by the 3rd this invention, and time-axis expanding of it was carried out is carried out, The write-in address generation circuit 12 which writes in the memory 11 and supplies an address signal, The read-out address generation circuit 13 which reads to memory 11 and supplies an address signal, Carry out reading appearance, write in an address signal, and it compares with the write-in address signal from a address generation circuit 12. reading appearance -- carrying out -- a address generation circuit 13 -- The comparison circuit 14 which reads so that the read-out address may write in and the address may not be crossed, and controls a address generation circuit 13, Carry out reading appearance, write in an address signal, and it compares with the write-in address signal from a address generation circuit 12. reading appearance -- carrying out -- a address generation circuit 13 -- It has the time delay convergence circuit 15 which reads so that the read-out address may write in and the address may be approached, and controls a address generation circuit 13.

[0016] According to this 3rd this invention, by the comparison circuit 14, write in the read-out address signal from the read-out address generation circuit 13, and it compares with the write-in address signal from a address generation circuit 12. While it reads so that the read-out address may write in and the address may not be crossed, and controlling a address generation circuit 13 It reads so that the read-out address signal from the read-out address generation circuit 13 may be written in, the read-out address may write in as compared with the write-in address signal from a address generation circuit 12 and the address may be approached, and a address generation circuit 13 is controlled by the time delay convergence circuit 15.

[0017] The 4th this invention is set to the 3rd this invention. The time delay convergence circuit 15 The subtractor 16 which reads from the write-in address signal of the write-in address generation circuit 12, and subtracts the address signal from a address generation circuit 13, When the output of the predetermined period above-mentioned subtractor 16 is forward based on the output from the positive/negative decision circuit 17 which makes a predetermined period judgment of the positive/negative of the output of the subtractor 16, and its positive/negative decision circuit 17, The initial address of the read-out address generation circuit 13 is set as the predetermined address which consists of this size.

[0018] The memory 11 to which repeat reading appearance of the data of two or more channels with which the data of two or more channels were repeatedly written in one by one, and, as for the time-axis expanding equipment by the 5th this invention, time-axis expanding was carried out is carried out one by one, Two or more write-in address generation circuits 12A-12D which generate the write-in address

signal in every two or more channels, and are supplied to memory 11, The maximum write-in address generation circuit 20 which generates the maximum write-in address signal for every round of two or more channels among each write-in address of two or more write-in address generation circuits 12A-12D, Reading appearance is carried out. reading appearance is carried out, an address signal is generated, and memory 11 is supplied -- with a address generation circuit 13 The read-out address signal from the read-out address generation circuit 13 is compared with the maximum write-in address signal from the maximum write-in address generation circuit 20. It has the address comparison circuit 21 which reads so that the read-out address may not cross the maximum write-in address, and controls a address generation circuit 13.

[0019] According to the 5th this invention of the above-mentioned ****, as compared with the maximum write-in address signal from the maximum write-in address generation circuit 20, the read-out address signal from the read-out address generation circuit 13 is read so that the read-out address may not cross the maximum write-in address, and a address generation circuit 13 is controlled by the comparison circuit 21.

[0020] The time-axis expanding equipment by the 6th this invention is a comparison circuit 21 in the 5th this invention. Carry out reading appearance and an address signal is compared with each write-in address signal from two or more write-in address generation circuits 12A-12D. reading appearance -- carrying out -- a address generation circuit 13 -- When the read-out address of the above-mentioned read-out address generation circuit 13 crosses one write-in address of two or more write-in address generation circuits 12A-12D The write-in address signal is read and the change circuit 22 which carries out change supply is established in memory 11 as an address signal.

[0021] According to this 6th this invention, the read-out address signal from the read-out address generation circuit 13 is compared with each write-in address signal from two or more write-in address generation circuits 12A-12D in a comparison circuit 21. When the read-out address of the above-mentioned read-out address generation circuit 13 crosses one write-in address of two or more write-in address generation circuits 12A-12D, by the change circuit 22 reading appearance -- carrying out -- instead of [of an address signal] -- the -- reading appearance was carried out and it was exceeded by the address -- it writes in and change supply of the write-in address signal of the address is carried out at memory 11.

[0022]

[Example] Below, with reference to drawing 1 , the transmission approach of the digital video signal by this invention and a digital audio signal and the example of transmission equipment are explained. In drawing 1 , between the transmitting section T and a receive section R is connected with one coaxial cable (BNC cable) 5.

[0023] The configuration of the transmitting section T is explained. The digital video signal (sampled with the frequency Fsc 4 times the frequency of a chrominance subcarrier and about 14.3MHz clock signal) from digital VTR is supplied to a mixer 3. the digital audio signal sampled with the 48kHz (a period is 20.83microsec) clock signal as shown in drawing 2 R> 2 -- the time-base-compaction circuit 2 -- supplying -- the horizontal synchronization chip period in the level period (63.55microsec) of a digital video signal -- 4 -- or time base compaction is carried out so that three samples may be inserted, a mixer 3 is supplied, and it mixes to a digital video signal. After the digital video/audio signal from a mixer 3 are supplied to the parallel/serial-conversion circuit 4 and changed into a serial digital video / audio signal, it is transmitted to a receive section R through one coaxial cable 5.

[0024] The configuration of a receive section R is explained. An eliminator 7 is supplied and it separates into a digital video signal and the digital audio signal by which time base compaction was carried out, after supplying the serial digital video / audio signal transmitted through the coaxial cable 5 from the transmitting section T to a serial / parallel-conversion circuit 6 and changing into a juxtaposition digital video / audio signal. The separated digital video signal is supplied to digital VTR 9 as it is. As shown in drawing 2 , after supplying the digital audio signal by which time base compaction was carried out to the time-axis expanding circuit 8 and returning it to the original digital audio signal, it is supplied to digital VTR 9.

[0025] According to the transmission approach of the digital video signal of this drawing 1 , and a digital audio signal, and transmission equipment, a digital video signal and a digital audio signal can be simultaneously transmitted with one cable.
[0026] Below, with reference to drawing 3 , the example (1) of the time-axis expanding equipment (circuit) by this invention is explained. the write-in address signal from the write-in address generation circuit (address counter) 12 is supplied to memory 11, the digital audio signal by which time base compaction was carried out is written in memory 11, reading appearance is carried out to the memory 11, reading appearance is carried out from a address generation circuit (address counter) 13, an address signal (the address change frequency of 1 for a predetermined number of the address change frequency of a write-in address signal with changing address signal) is supplied, and the digital audio signal of the origin by which time-axis expanding was carried out from the memory 11 is read.
[0027] Since the window of this memory 11 is 16 lines of a digital video signal here, the address of the write-in address generation circuit 12 is cleared once for every 16 lines of a digital video signal. In this case, the address of the read-out address generation circuit 13 is cleared after counting up to the write-in address in front of a clearance.
[0028] an address comparison and reading appearance -- carrying out -- counting of the address -- a control circuit 14 Carry out reading appearance, and when [of a address generation circuit 13] carry out reading appearance, and write in an address signal, reading appearance is carried out as compared with the write-in address signal from a address generation circuit 12, the address writes in and the address is not crossed, a count-up signal is generated. Supply a address generation circuit 13, this is read, when the read-out address is made to increase or clear and is crossed, it is made not to generate a count-up signal, it reads by this, and the address of a address generation circuit 13 does not change, but maintains a fixed address value.
[0029] reading appearance of the delay convergence circuit 15 is carried out, when [of a address generation circuit 13] carry out reading appearance and an address signal is written in, the 16 field carries out between reading appearance, the address writes in [the write-in address signal from a address generation circuit 12] and the address is not crossed, as shown in drawing 4 , reading appearance of it is carried out immediately after a clearance, and it gives adult offset, i.e., the 1st street, from this to the address (0th street). Namely, if write in with a subtractor 16, read from the address, the address is subtracted, the subtraction output is supplied to the positive/negative decision circuit 17 and forward is maintained for the 16 field, the load value generating circuit 18 will be controlled. By loading a value to which only the last bit sets the initial value oar 0 of the address counter of the read-out address generation circuit 13 to 1, and repeating this reading appearance can be carried out, the address approaches the write-in address, and reading appearance of it can be carried out and it can make small the amount of delay to the write-in address of the address.
[0030] According to this time-axis expanding equipment, after not making the window of memory 11 not much small also writes data in memory, a time delay until it reads the data by which time-axis expanding was carried out can be shortened.
[0031] Next, with reference to drawing 5 , the example (2) of the time-axis expanding equipment (circuit) of this invention is explained. It is written in by the write-in address signal from the write-in address registers (an address counter is also good) 12A-12D with which the audio data by which time base compaction was carried out are supplied to memory 11, and are supplied to memory 11, and reading appearance of the audio data by which time-axis expanding was carried out is carried out through a selector 22 by the read-out address signal from the read-out address register 13 supplied to memory 11.
[0032] Although expressed with a binary code, since it is easy, when both the write-in address and the read-out address express these addresses with a decimal sign, they change as follows. In addition, the most significant digit of this address shows the exception of a channel.
the write-in address of one channel 100001, 100002, 100003, and ..... the write-in address of two channels 200001, 200002, 200003, and ..... the write-in address of three channels 300001, 300002, 300003, and ..... the write-in address of four channels [400001, 400002, 400003, and ..... 0033] With

and the data CH1 and CH2 with which the AUX data shown in drawing 6 are supplied to the channel recognition circuit 19, and express the channel of the bits 1 and 2 of the cutting tool 0 in the user data (audio data) UD It recognizes any of four channels the samples of the digital audio data by which time base compaction was carried out are. It responds to the recognized channel. One by one 1, 2, 3, and four-channel write-in address register 12A, Make it increase every [1], or clear the address of the address signal from 12B, 12C, and 12D, and the address signal of the channel of each of those registers 12A-12D is supplied to memory 11. Each sample data of digital audio data is written in the address for every channel of memory 11. In addition, for head discernment data and DID, in AUX data, Data ID (the number of blocks is shown) and DBN are [ADF / a data counter (the magnitude of UD is shown) and CS of a data block number and DC] termination data.

[0034] Moreover, supply the address signal supplied to memory 11 from the write-in address registers 12A-12D of each channel to the maximum address register 20, the maximum address of the write-in address of one to four channels is made to hold, and it gets to know of what sample digital audio data have been transmitted at the event of the last of one line of a digital video signal.

[0035] For example, the address of the memory of the sample of each channel of the digital audio signal (data) which is inserted in the horizontal synchronization chip period of the digital video signal of a certain line and by which time base compaction was carried out is one channel. 1000672 channels 2000603 channels 3000604 channels In the case of 400060, the maximum write-in address turns to 100067 which is the address of one channel. In addition, the top digit to which the maximum write-in address expresses the exception of a channel in this case shall ignore.

[0036] And the address comparator 21 compares the read-out address from the read-out address register 13 with the maximum write-in address of the maximum write-in address register 20. When the read-out address does not cross the maximum write-in address when carry out reading appearance, reading appearance of the count-up signal is supplied and carried out to an address register 13, it increased or clears and the address is crossed, a count-up signal is not generated, but by this, reading appearance is carried out and the address of an address register 13 is maintained to constant value. The address signal from the read-out address generation circuit 13 is supplied to memory 11 through the selector 22 controlled by the select signal from the address comparator 21.

[0037] By the address comparator 21, moreover, the read-out address signal from the read-out address register 13 Respectively 1, 2, 3, and the four-channel write-in registers 12A and 12B, When the read-out address crosses either 1, 2, 3 or the write-in address of four channels as compared with the write-in address signal of 12C and 12D A selector 22 is controlled by the comparison output from the address comparator 21, and the write-in address signal exceeded by the read-out address is supplied to memory 11 through a selector 22 instead of the read-out address signal from the read-out address register 13. .

[0038] (I) of drawing 7 (II) (III), and (IV) -- the write-in address from 1, 2, 3, and the four-channel write-in address registers 12A, 12B, 12C, and 12D, and reading appearance -- carrying out -- the reading appearance from an address register 13 -- carrying out -- the change condition of the address -- being shown -- drawing 8 -- the maximum write-in address of the maximum write-in address register 20 -- and reading appearance is carried out, an address register 13 carries out reading appearance, and the change condition of the address is shown. In addition, both the high-order digits to which this address expresses the exception of a channel are shown as what comes out zero.

[0039] (I) of drawing 7 (II) (III), And it is shown that A period each of drawing 8 had all four reception of this measurement size in the (IV) list, the period of B shows a period with all four lack of received data, and, as for after Periods A and B, the defect state of the received data of 2 and four channels continues. by carrying out reading appearance, as shown in drawing 8 , although reading appearance is carried out in the range from an address register 13 which does not exceed the maximum write-in address from the maximum write-in address register 20 and the address increases, in the period of C which the increment in the maximum write-in address stopped by lack of received data, reading appearance of the address is carried out and it also stops [carry out / reading appearance] the increment in the address. Drawing 7 (I) It reaches (III). Since reception of the sample data of 1 and three channels is started in the period of D after the period of C so that it may be shown, the read-out address of the

read-out address register 13 increases again. Then, since a clearance of 1 time per 16 lines of the write-in address to a digital video signal arises, after the read-out address increases to the address in front of the clearance of the maximum write-in address, it is cleared, and both the addresses increase again.
[0040] As shown in drawing 7 (II) and (IV), moreover, the read-out address of the read-out address register 13 In the period of D which passes each write-in address of 2 and the four-channel write-in address registers 12B and 12D Since it turns to reading unsuitable sample data when a read-out address signal is then supplied to memory 11 Each write-in address signal of 2 and the four-channel write-in address registers 12B and 12D is read, and it is made to supply memory 11 as an address signal by the change of a selector 22.
[0041] Thereby, the continuity of data is securable also to the channel which lacks received data. Moreover, the write-in address of the write-in address register of a channel with which a sample was not transmitted at all among four channels is the 0th ****. then, when all bits wrote 0 and the data which change in the 0th street of memory 11 beforehand, the write-in address of the channel which carries out reading appearance and which has been made into the address is adopted and the 0th street of the write-in address of the channel is read, the receiving sample of the channel turns to reading appearance of the sample data of all the bits 0 always being carried out. Although the address for every channel of the read-out address register 18 changes with the 0th street immediately after a clearance for every channel, respectively Data will be read in the 1st street of the channel of memory 11 if one sample also receives the data of a certain channel. Since reading appearance of the 0th street to the sample data of the channel of memory 11 is carried out only when the data of a channel are zero sample, the voice output of the channel is the same as having grown into the mute condition substantially as a result.
[0042] In the time-axis expanding equipment with which according to the above-mentioned **** time-axis expanding equipment the digital audio signal of two or more channels is supplied, and the digital audio signal of two or more channels by which time-axis expanding was carried out is outputted Even if it lacks a part of sample of the digital audio signal of two or more channels or sequence is wrong, while being able to perform smoothly control of a write-in address register and a read-out address register Since the required data memorized by memory can be certainly read even if the increment in the maximum write-in address of a maximum write-in address counter stops, the continuity of data can be maintained and the time-axis expanding equipment which can perform the faithful rendering of received data can be obtained.
[0043] Although the time-axis expanding equipment (circuit) of each example mentioned above consists of semiconductor ICs, it may consist of discrete circuits.
[0044]
[Effect of the Invention] According to the 1st and 2nd this inventions of the above-mentioned ****, the transmission approach of of the digital video signal and digital audio signal which can transmit simultaneously a digital video signal and a digital audio signal, and transmission equipment can be obtained using one cable.
[0045] According to the 3rd this invention of the above-mentioned ****, even if it does not make a window not much small, after writing data in memory, the time-axis expanding equipment which can shorten a time delay until it reads the data by which time-axis expanding was carried out can be obtained.
[0046] According to the 4th this invention of the above-mentioned ****, in the time-axis expanding equipment with which the digital audio signal of two or more channels is supplied, and the digital audio signal of two or more channels by which time-axis expanding was carried out is outputted, even if it lacks a part of sample of the digital audio signal of two or more channels or sequence is wrong, what can perform smoothly control of a write-in address register and a read-out address register can be obtained.
[0047] In the time-axis expanding equipment with which according to the 5th this invention of the above-mentioned **** the digital audio signal of two or more channels is supplied, and the digital audio signal of two or more channels by which time-axis expanding was carried out is outputted Even if it lacks a part of sample of the digital audio signal of two or more channels or sequence is wrong, while being able to perform smoothly control of a write-in address register and a read-out address register

Even if the increment in the maximum write-in address of a maximum write-in address counter stops, the time-axis expanding equipment which can obtain certainly the required data memorized by memory can be obtained.

[0048] In the time-axis expanding equipment with which according to the 6th this invention of the above-mentioned **** the digital audio signal of two or more channels is supplied, and the digital audio signal of two or more channels by which time-axis expanding was carried out is outputted Even if it lacks a part of sample of the digital audio signal of two or more channels or sequence is wrong, while being able to perform smoothly control of a write-in address register and a read-out address register Since the required data memorized by memory can be certainly read even if the increment in the maximum write-in address of a maximum write-in address counter stops, the continuity of data can be maintained and the time-axis expanding equipment which can perform the faithful rendering of received data can be obtained.

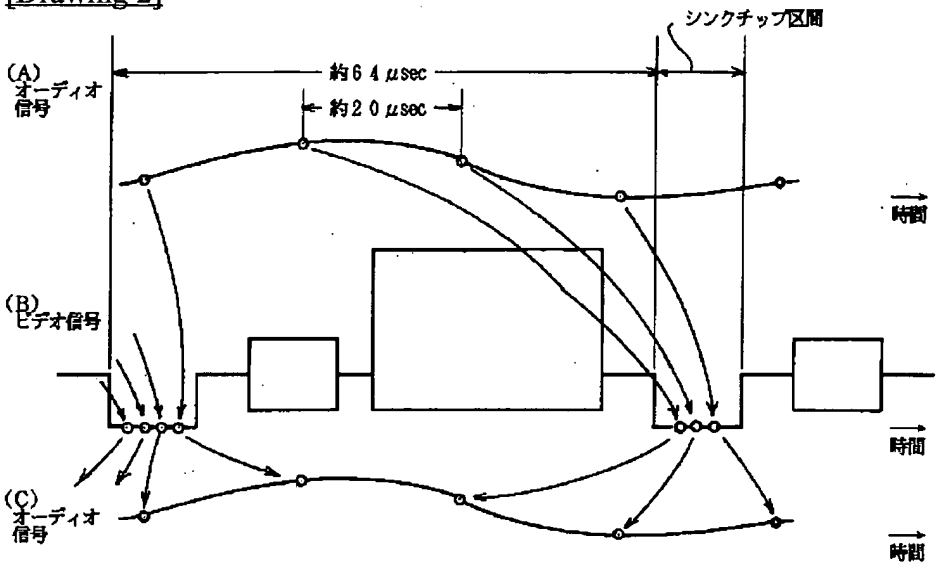
[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

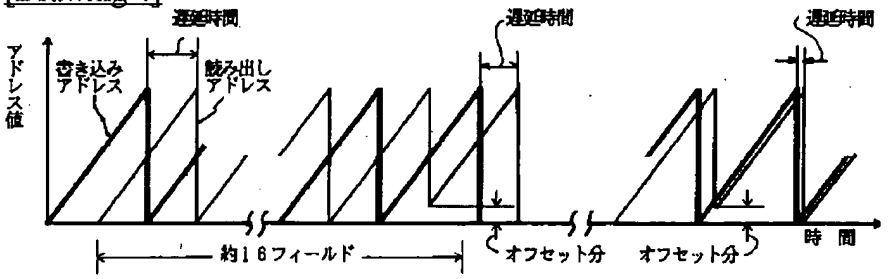
DRAWINGS

[Drawing 2]



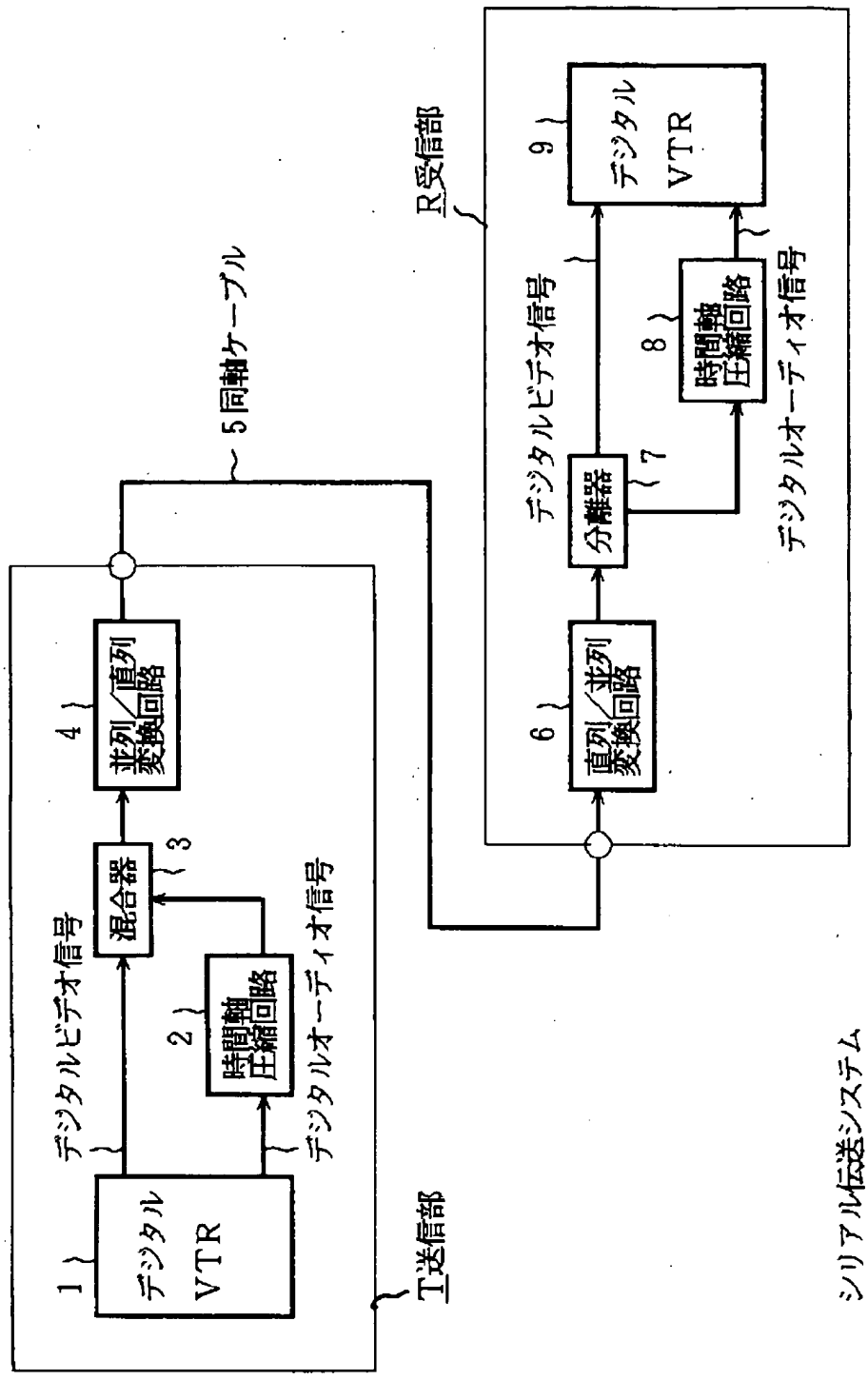
オーディオ信号の時間圧縮及び伸長

[Drawing 4]

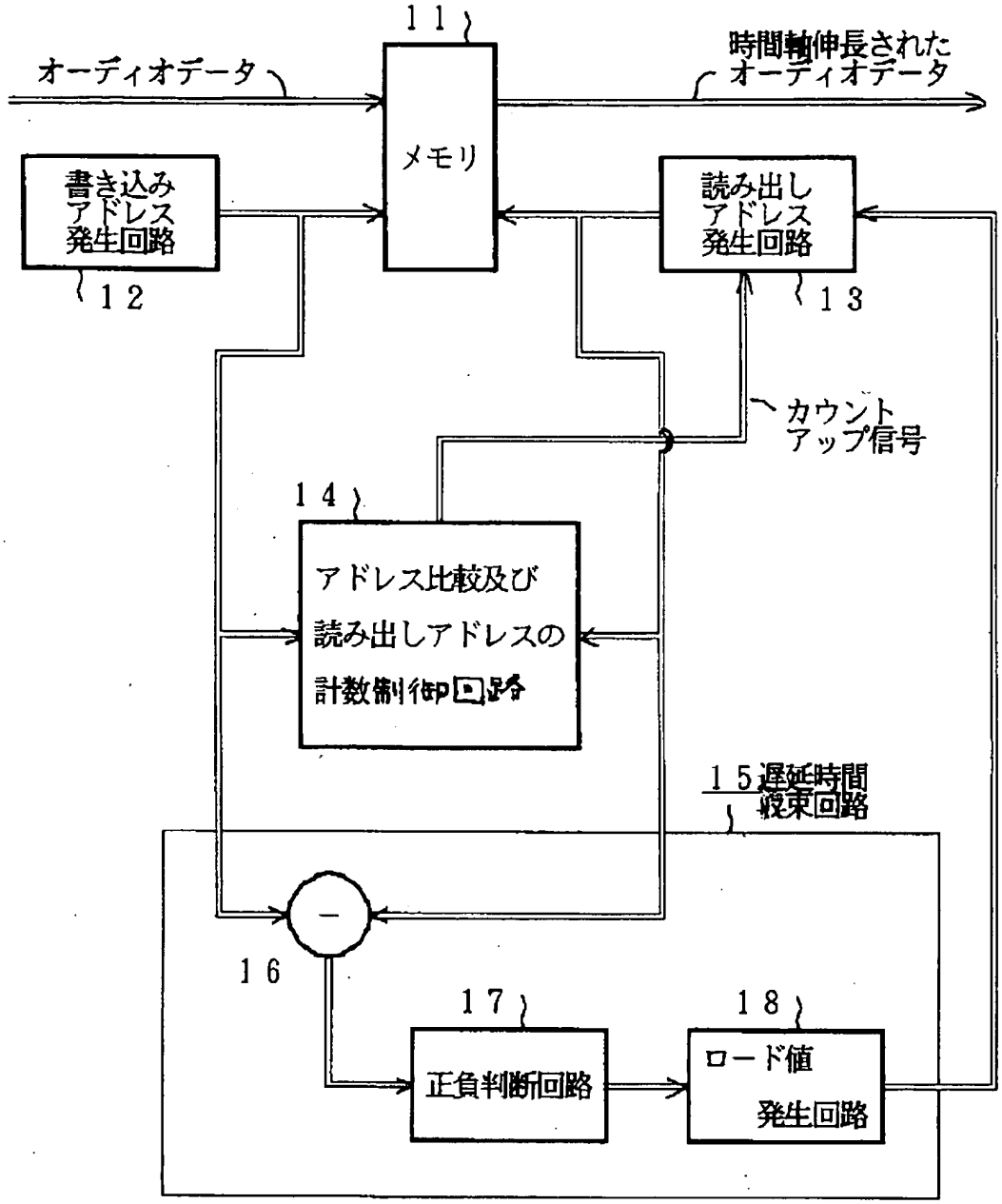


書き込みアドレス及び読み出しアドレスの関係

[Drawing 1]

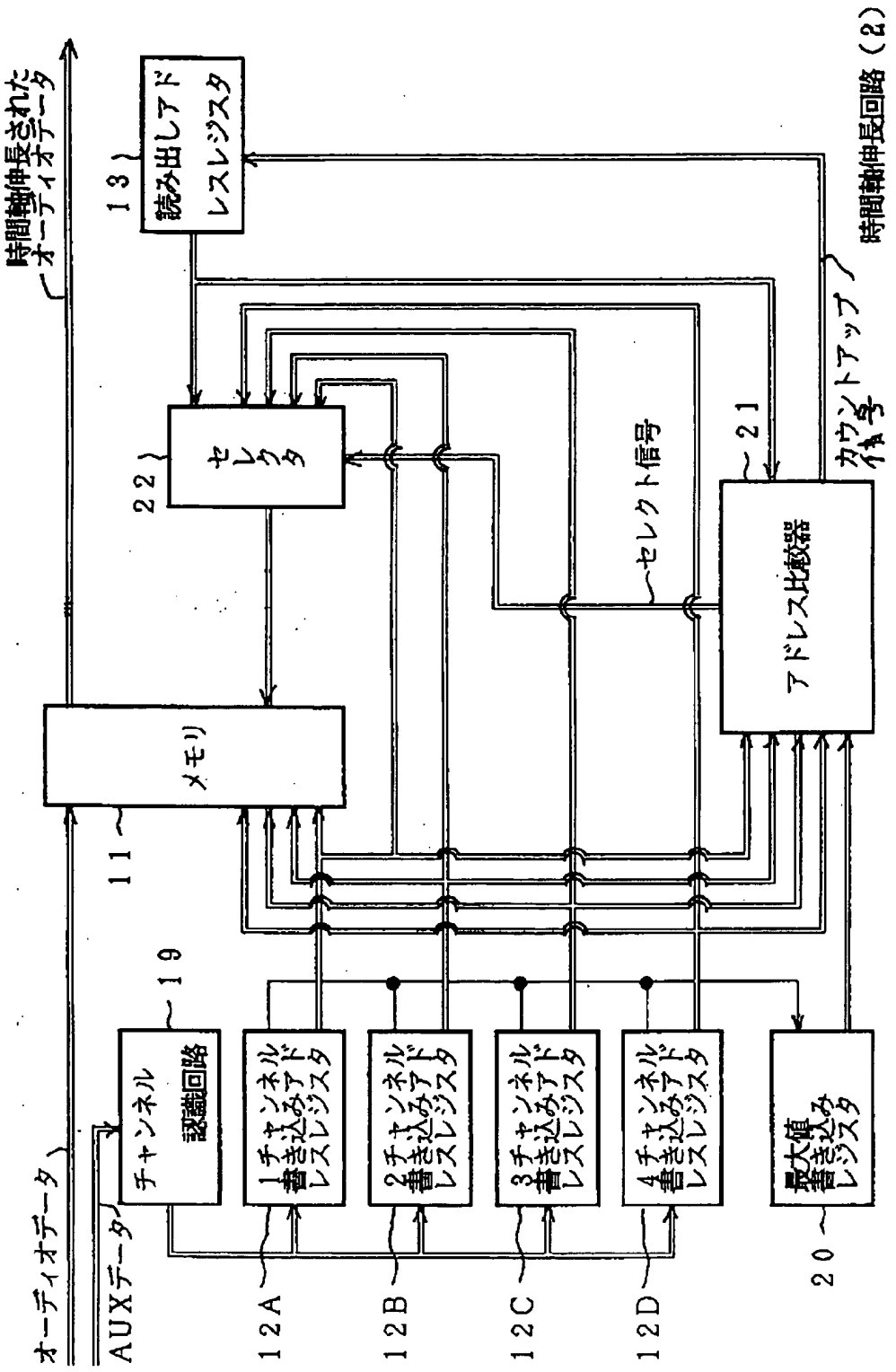

T送信部
R受信部
1
デジタル VTR
デジタルビデオ信号
デジタルオーディオ信号
2
時間軸圧縮回路
3
混合器
4
並列／直列変換回路
5同軸ケーブル
6
直列／並列変換回路
7
分離器
8
時間軸圧縮回路
9
デジタル VTR
デジタルビデオ信号
デジタルオーディオ信号
シリアル伝送システム

[Drawing 3]

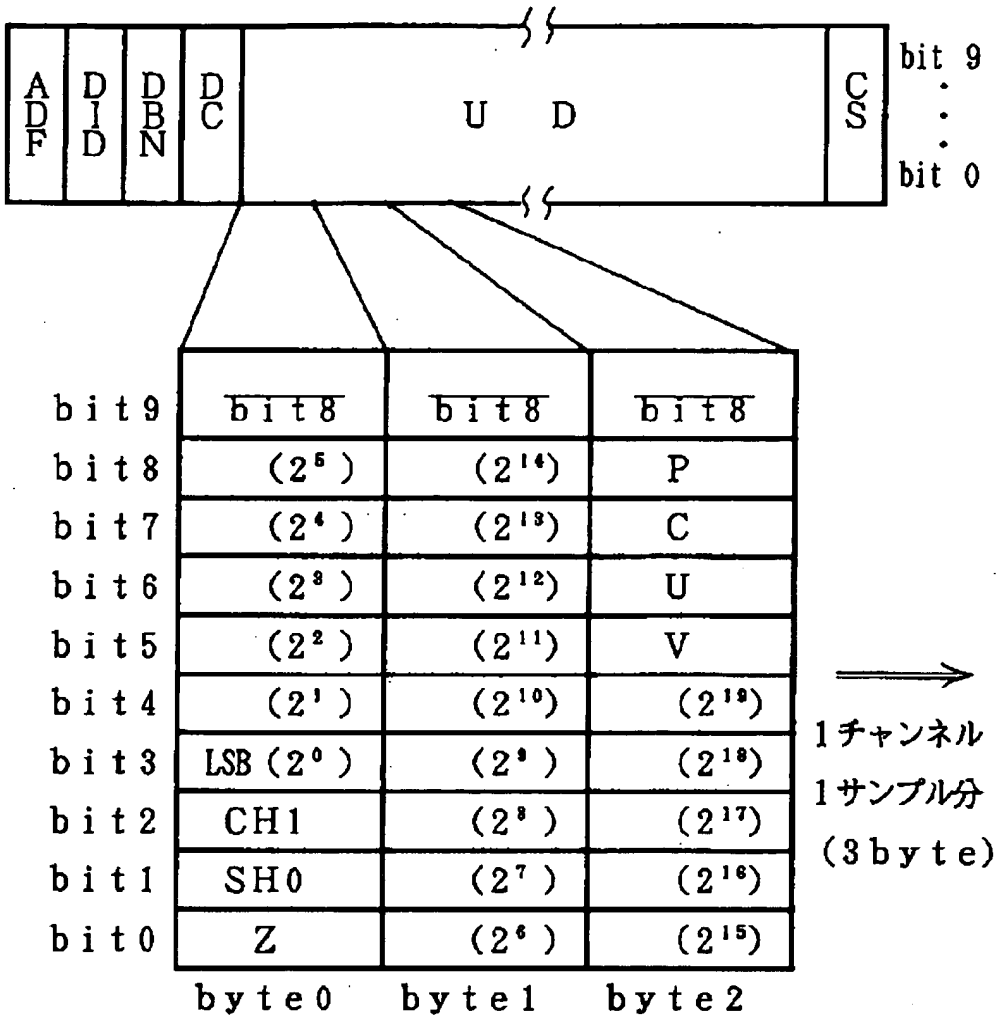


時間軸伸長回路（1）

[Drawing 5]

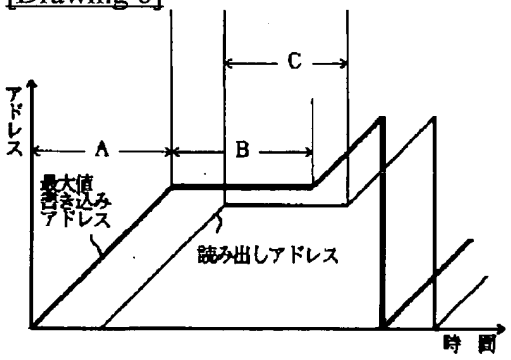

時間軸伸長されたオーディオデータ
13
読み出しアドレスレジスタ
時間軸伸長回路（2）
カウントアップ信号
21
アドレス比較器
22
セレクタ
セレクト信号
メモリ
11
19
チャンネル認識回路
1チャンネルアドレスレジスタ
2チャンネルアドレスレジスタ
3チャンネルアドレスレジスタ
4チャンネルアドレスレジスタ
最大値書き込みレジスタ
20
オーディオデータ
AUXデータ
12A
12B
12C
12D

[Drawing 6]



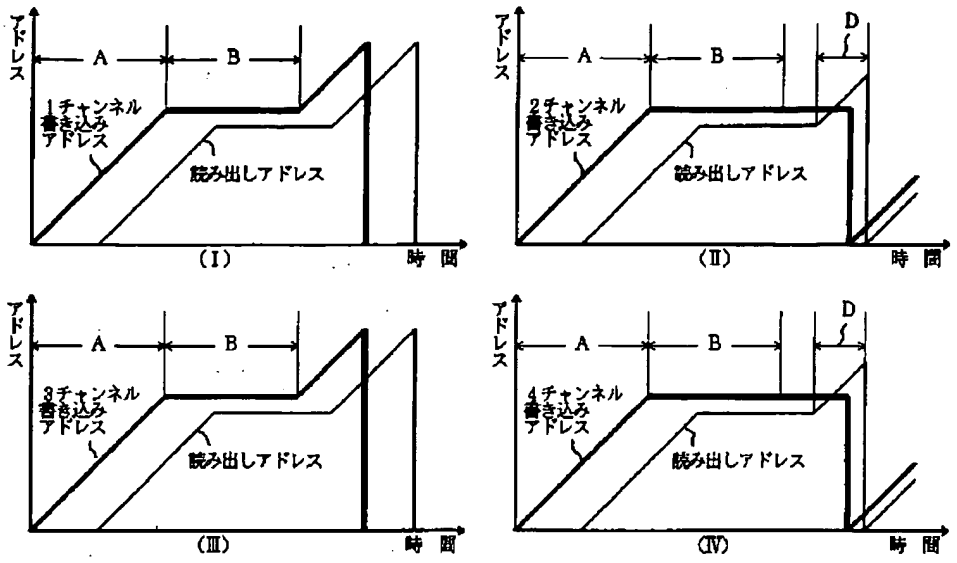
AUX データフォーマット

[Drawing 8]



メモリの書き込みアドレス及び読み出しアドレスの関係

[Drawing 7]



メモリの読み出しアドレス及び書き込みアドレスの関係

[Translation done.]